WHAT IS CLAIMED IS:

1. A method of forming an array of microelectronic elements, said method comprising the steps of:

a) preparing a first wafer of semiconductor material by implanting, through a first surface of said first wafer, ions to a planar region at a selected depth therein, said ions being ions of an element selected from hydrogen and the noble gases,

b) preparing a second wafer of semiconductor material, said second wafer comprising a layer of dielectric material having a second surface, a pattern of mutually electrically isolated metal conductors being disposed within said layer, said metal conductors comprising spaced apart conducting regions extending to and being exposed at said second surface,

c) placing said first wafer over said second wafer with said first surface of said first wafer in juxtaposed adherence and electrical contact with said second surface and with said conducting regions exposed thereat, and

d) inducing a fracture along said planar region of said first wafer to leave a semiconductor layer of said first wafer defined/bounded between said first surface and a fracture surface formed in said planar region, said first surface remaining in electrically contacting adherence with said second surface.

2. A method as set forth in Claim 1 wherein step a) comprises a further step of forming a semiconductor device in said semiconductor layer above each of said conducting regions of said metal conductors.

3. A method as set forth in Claim 2, wherein said microelectronic elements are magnetoresistive memory elements, said method comprising the further step of forming an MTJ structure in electrical contact with said semiconductor layer above each of said conducting regions of said metal conductors.

4. A method as set forth in Claim 3, said semiconductor device being a diode and said magnetoresistive memory element being in electrical contact therewith.

5. A method as set forth in Claim 4, wherein said magnetoresistive memory element comprises an MTJ structure.

6. A method as set forth in Claim 1, wherein step a) comprises a further step of forming a field effect transistor at positions in said semiconductor layer which overlie said conducting regions of said metal conductors, each of said conducting regions serving as a first gate electrode of said field effect transistor.

7. A method as set forth in Claim 6, wherein step a) comprises a further step of forming a first oxide layer on said first surface of said first wafer before step c) .

8. A method as set forth in Claim 7, comprising a further step of forming a second oxide layer on said fracture surface.

9. A method as set forth in Claim 8, wherein a second gate electrode overlies said second oxide layer above each said field effect transistor.

10. A method as set forth in Claim 9, wherein each said conducting region is a metal-filled via.

11. An array of microelectronic elements comprising:

a) a substrate of semiconductor material,

b) a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto,

c) a pattern of mutually electrically isolated metal conductors disposed within said lower layer of dielectric material, said metal conductors comprising a plurality of spaced apart conducting regions extending to said upper surface of said lower layer,

d) an upper layer of delectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer, and

e) a plurality of nodes of oriented single crystal grain, monocrystalline, semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer.

12. An array as set forth in Claim 11, each of said nodes comprising a semiconductor device.

13. An array as set forth in Claim 11, each of said nodes comprising a diode.

14. An array as set forth in Claim 13, wherein said microelectronic elements comprise magnetoresistive memory elements each comprising a said diode and an MTJ structure.

15. An array as set forth in Claim 12, wherein said semiconductor device is a field effect transistor comprising a first gate electrode in contact with one of said conducting regions at said upper surface of said lower layer

16. An array as set forth in Claim 12, wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer, and wherein a second gate electrode is deposited upon said first insulating layer above each field effect transistor.

17. An array as set forth in Claim 11, wherein said oriented single crystal grain semiconductor material is oriented in the <100> orientation.

18. An array as set forth in Claim 11, wherein each conducting region comprises a via filled with electrically conducting material.